

SYS-102 Basic Computer Architecture
Assessment Activity SYS-102:00060
State Machine Design

Name: (Win) Thanawin Pattanaphol

Student ID: 01324096

Counter Circuit

A counter circuit counts in binary up to a maximum value (according to its number of bits) and resets to zero and counts up again.

2 D Flips flops can store up to **4 unique states**, thus, it means that the counter will reset after every 4 iterations.

The truth table below demonstrates how states are updated in relation to the clock signals – 8 clock signal example:

Clock Pulse	Q₀	Q₁	D₀ / Q₀'	D₁ / Q₁'
0	0	0	1	1
1	1	1	0	0
0	1	1	0	0
1	0	1	1	0
0	0	1	1	0
1	1	0	0	1
0	1	0	0	1
1	0	0	1	1

Truth table consisting of state changes that occurs when clock signal goes from 0 to 1 with comparison to the values that will occur in the next cycle.

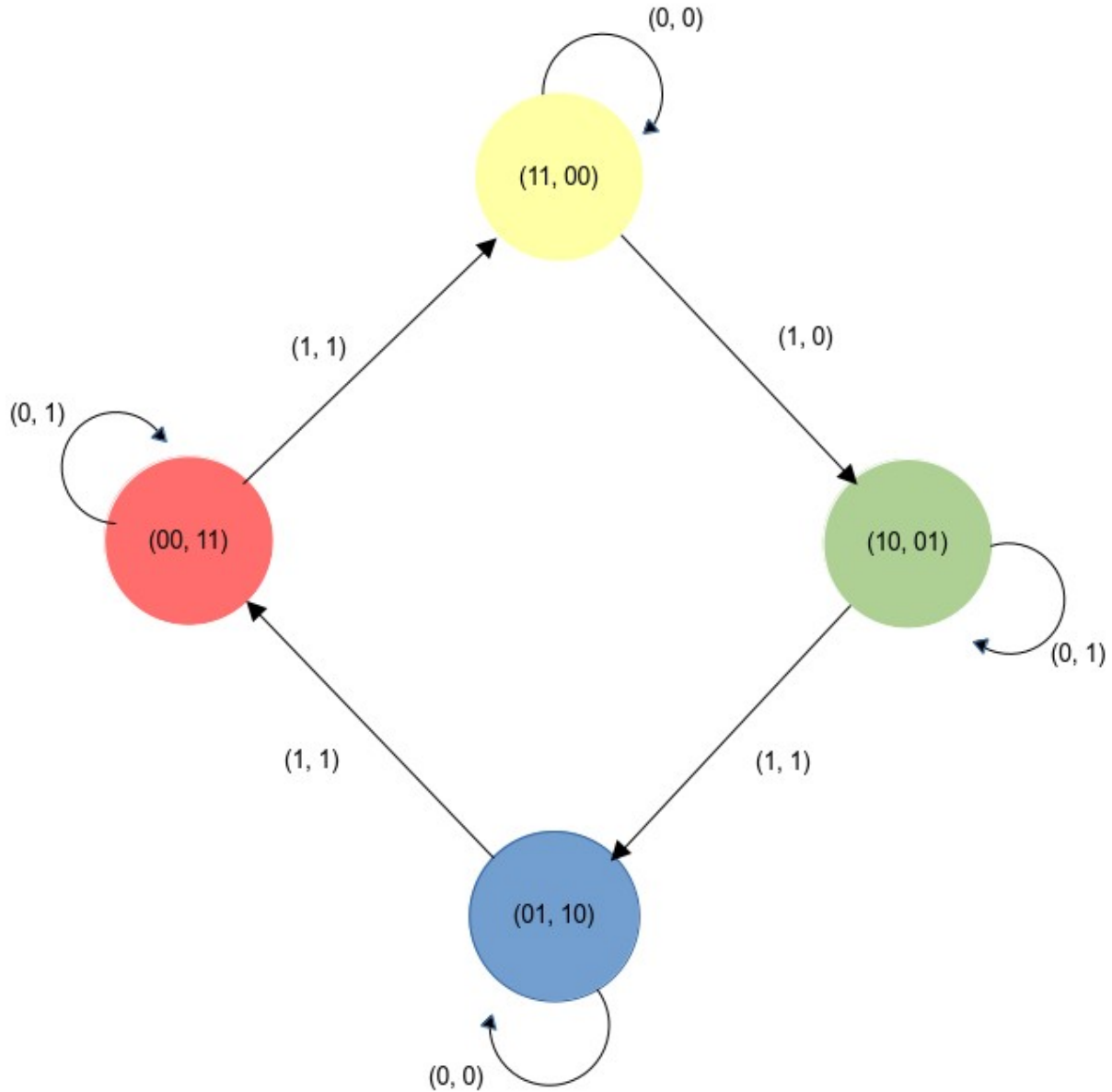
Present State				Next State	
Q₀	Q₁	D₀ / Q₀'	D₁ / Q₀'	Q₀	Q₁
0	0	1	1	1	1
1	1	0	0	0	1
0	1	1	0	1	0
1	0	0	1	0	0

We can observe that the next state values of Q₀ and Q₁ corresponds to the values of the following present state values, which, we can use them to make a state diagram.

**SYS-102 Basic Computer Architecture
Assessment Activity SYS-102:00060
State Machine Design**

Name: (Win) Thanawin Pattanaphol

Student ID: 01324096



State diagram for the counter circuit

SYS-102 Basic Computer Architecture
Assessment Activity SYS-102:00060
State Machine Design

Name: (Win) Thanawin Pattanaphol

Student ID: 01324096

7 segment display decoder

A 7 segment display decoder circuits converts binary inputs into outputs that turns on specific parts of the display.

$$A = Q_1' + Q_0$$

$$B = Q_1' + Q_0'$$

$$C = Q_0'$$

$$D = Q_1 \text{ XNOR } Q_0$$

$$E = 1$$

$$F = Q_1 + Q_0$$

$$G = Q_1' + Q_0'$$

Here, we can see that most decoders takes at most two inputs from the counter states and are already at their most simplified state – no simplicated needed. These decoders can be divided into different categories.

1. C segment gets its value directly from Q0
2. E segment will always be on as its value is one
3. A, B, F, and G segments get their value from the OR gates.
4. D gets its value from an XNOR gate.

As the logic for each segment has been identified, a truth table can now be constructed to identify the values for each state transition. Each state is represented in the form (Q_1 , Q_0 and Q_1' , Q_0')

State	A	B	C	D	E	F	G
(00, 11)	1	1	1	1	1	0	1
(11, 00)	1	0	0	1	1	1	1
(10, 01)	0	1	1	0	1	1	0
(01, 10)	1	1	0	0	1	1	1

Taken from the truth table, we can visualize it on a 7-segment display as below.

SYS-102 Basic Computer Architecture
Assessment Activity SYS-102:00060
State Machine Design

Name: (Win) Thanawin Pattanaphol

Student ID: 01324096

