

# Assessment 2

This is the second assessment for SYS102: Basic Computer Architecture (Fall 2024). The assessment covers state machine design. The total score before weighing is 100.

## State machine design

### Instructions:

You are provided with a sequential circuit that includes two **D flip-flops** and a set of logic gates as in Figure 1. The outputs from this circuit are intended to drive a **7-segment display** labeled with segments **A** through **G** as in Figure 2. Your task is to:

#### 1. State Transitions (Truth Table):

- Derive the **truth table** for the two D flip-flops ( $Q_1, Q_0$ ) showing the current state and the next state after each clock pulse.

#### 2. State Diagram:

- Draw a **state diagram** showing the transitions between states based on the clock signal. Label each state and the corresponding transitions between them.

#### 3. 7-Segment Display Logic:

- Analyze how the logic gates determine the behavior of the 7-segment display for each segment A through G.
- Use Boolean algebra (or another method) to express the conditions under which each segment is turned on or off.

#### 4. 7-Segment Decoder Logic:

- a. Based on your analysis, explain how the flip-flop outputs control the segments of the 7-segment display to show specific information.
- b. Derive Boolean equations for segments A through G.

### Assessment Deliverables:

- Completed **truth table** showing the state transitions of the D flip-flops.
- A clear **state diagram** that illustrates the transitions between states.
- **Boolean expressions** or **explanations** for how each segment of the **7-segment display** is controlled by the flip-flop outputs.
- Explanation of how the 7-segment display will behave for different states of the flip-flops.

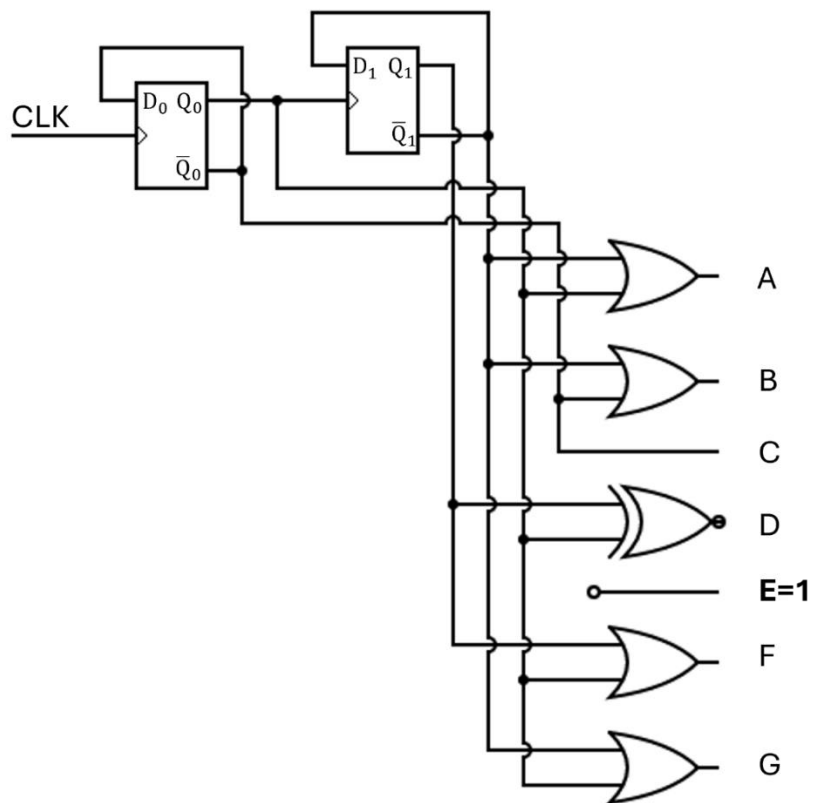


Figure 1: Sequential circuit that includes two D flip-flops and a set of logic gates

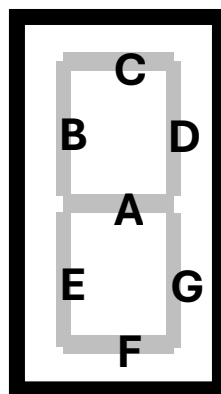


Figure 2: 7-segment display labeled with segments A through G

### Grading Criteria:

- **Truth Table** (30%): Accurate derivation of the truth table and correct state transitions.
- **7-Segment Logic** (30%): Clear and correct Boolean equations or explanations showing how segments A through G are controlled.
- **State Diagram** (30%): Correct and clear representation of the state transitions.
- **Explanation** (10%): Clarity of explanation and reasoning for the circuit's behavior.